NASA-DOD Lead-Free Electronics (Project 2)

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Background

NASA's earlier lead-free solder high-reliability testing effort helped shed light on the reliability of circuit cards manufactured with lead-free solders. However, that project was not able to fully explore rework and solder mixing. As the transition to lead-free becomes an ever-closer reality for military and aerospace applications, it will be critical to fully understand the implications of rework and solder mixing.

This joint project of DoD, NASA and defense and space contractor representatives will build on the results from the former NASA-led lead-free solder project. The new effort will focus on the rework of tin-lead and lead-free solder alloys and will include the mixing of tin-lead /lead-free & lead-free/ tin-lead solder alloys.

Objective

In response to concerns about risks from lead-free induced faults to high reliability products, NASA has outlined a multi-year project to provide manufacturers and users with data to clarify the risks of lead-free materials in their products. The project will also be of potential interest to component manufacturers supplying to high reliability markets. The project was launched in November 2006. The primary technical objective of the project is to undertake comprehensive testing to generate information on failure modes/criteria to better understand the reliability of packages (e.g., Thin Small Outline Package, Ball Grid Array, Plastic (Dual Inline Package) assembled and reworked with lead-free alloys and with mixed (lead/lead-free) alloys.

The assembled boards will be subjected to accelerated testing (e.g., thermal, vibration) to understand solder joint reliability. Results from the project will be available during the duration of the project allowing advance information to assist organizations in their own implementation or mitigation strategies.

Period of Performance

November 2006 to September 2010

Stakeholders

NASA Centers (Kennedy Space Center, Jet Propulsion Laboratory, Marshall Space Flight Center, Johnson Space Center, Goddard Space Flight Center, Ames Research Laboratory), NASA contractors (United Space Alliance-Solid Rocket Booster, Boeing-Orbiter), major commercial and defense aerospace contractors (BAE Systems, Boeing, Lockheed Martin, Raytheon, Rockwell Collins), Air Force, Army, Navy, Marines, Dept. of Energy and other private entities.

Benefits

- Project will fast-track since it builds off of the previous NASA lead-free project
- Data generated from this project is required to gain a better understanding of how lead-free electronics will perform in high-reliability aerospace applications
- Even though NASA and the aerospace community are exempt from lead-free laws and regulations, there may not be enough suppliers available to meet needs
- Military and aerospace contractors are receiving unwanted electronics components with lead-free finishes.

Document Status

- Joint Test Protocol Final October 8, 2007 (NLFE Project JTP October-08-2007.pdf, 666KB, 36 pages, October 8, 2007)
- Project Plan Final November 17, 2008 (NASA-DoD LFE Project Plan Nov-17-2008.pdf, 9MB, 74 pages, November 17, 2008)

Recent Progress

- Test vehicle rework is currently in progress.
- Test vehicles being reworked by NSWC Crane have been completed and shipped to BAE Systems for thermal aging.

Milestones

- The Joint Test Protocol was finalized on October 8, 2007. JTP testing activities being coordinated include:
 - Thermal cycling: -20oC to +80oC
 - Thermal cycling: -55oC to +125oC
 - Vibration
 - Combined environments testing
 - Drop testing
 - Mechanical shock
 - Integrated stress testing
 - Copper dissolution.
- Test vehicle assembly was completed August 2008 by BAE Systems Irving, Texas

Near-Term Goals

- Receive Joint Test Protocol endorsement letters from all stakeholders
- Complete test vehicle rework

Presentations

- NASA-DoD Lead-Free Electronics Project (NASA_DoD LFE Project Details_Jul-17.pdf, 5 MB, 33 pages, July 17, 2008)
- Printed Trace Testing Report (Printed Trace Testing _Final.pdf, 629KB, 8 pages, March 16, 2008)
- Value-add Solutions for the BGA Supply Chain (Premier BGA Presentation 7-28-08.pdf, 669KB, 39 pages, July 28, 2008)

Additional Activities

Investigation of printed traces

The NASA-DoD Lead-Free Electronics Project is investigating printed trace technology as a possible rework procedure for printed wiring assemblies. The deposition or prototyping technologies used for creating printable electronics emerged from a Defense Advanced Research Projects Agency (DARPA) program titled Mesoscale Integrated Conformal Electronics (MICE). The program ran from 1998 through 2003 and developed a number of advanced direct write technologies. The Center for Accelerated Applications at the Nanoscale (CAAN) at the South Dakota School of Mines and Radiance Technologies are working to further refine the technologies for DoD applications.

- IST coupon Deposition brief February 12, 2008 (IST Coupon Deposition Test-Radiance.pdf, 646KB, 6 pages, February 12, 2008)
- Final Printed Trace Testing (Printed Trace Testing Final.pdf, 629KB, 8 pages, March 16, 2008)

New Mexico Tech Lead-Free Solder Research

The Microelectronics Testing and Technology Obsolescence Program (METTOP) is a small microelectronics testing and research facility located at New Mexico Tech, in Socorro, NM. The facility recently started a lead-free solder research program, to assist in mitigating Diminishing Manufacturing Sources and Material Shortages (DMSMS) issues and concerns regarding reliability-information, or the lack there of, on lead-free solders for use in Military and Aerospace applications. METTOP joined with Naval Surface Warfare Center (NSWC) Crane and Purdue University on their Project 1722-Impact of Lead-Free Components on Military Repair. The purpose of this project is to develop with NAVSEA Crane a technical team of industry, academia and military to evaluate existing data and recommend strategy for DOD on military electronics affected by the lead-free initiative. Emphasis is placed in four areas: tin whiskers, solder joint reliability, copper dissolution and cross-contamination. METTOP has focused on the issue of solder joint reliability, particularly in the area of vibration testing.

- New Mexico Tech Lead-Free Solder Research Paper (NMT_NASA_paper.pdf, 569KB, 62 pages, May 2008)
- New Mexico Tech Lead-Free Solder Research Presentation (NASA_NMT_presentation.pdf, 1MB, 30 pages, May 2008)

Completed Activities

Area Array X-Ray Analysis

Once test vehicle assembly was completed, all test vehicles were shipped to Lockheed Martin for x-ray analysis of the area array components, BGA and CSP. The QFN components were analyzed as well. Percentage of voiding as well as ball shape were documented.

Automated X-Ray of Circuit Card Assemblies (NASA-DoD Lead-Free Electronics Project X-Ray Results.pdf, 7 pages, 1MB)

Interconnect Stress Test (IST): PWB Interconnect Solutions Inc.

IST has the capability of effectively/rapidly quantify the integrity of both the Plated Through Hole (PTH) and the unique ability to identify the presence & levels of post separations within the multilayer board (MLB). IST both compliments and/or dramatically reduces the levels of microsection analysis required for PWB interconnect quality assessment.

The IST principles are unique in that they simultaneously quantify the integrity of both the PTH and its interconnections to the internal layers (posts) throughout accelerated stress testing. IST creates a uniform strain from within the substrate, the interconnects ability to

distribute and redistribute this strain provides an indication of integrity. The plated barrels and inner layer junctions are exercised until the initial failure mode/mechanism is uncovered.

- Thermal Distribution in an IST Coupon (Thermal Distribution in an IST Coupon.pdf, 464KB, 7 pages, April 29, 2008)
- NASA-DoD_IST Coupons_set-1 (NASA-DoD_IST Coupons_set-1.pdf, 2MB, 37 pages, March 28, 2008).

Updated: 12/31/08